REMARKS/ARGUMENTS

In the Office Action mailed August 3, 2007, claims 1-12 were rejected. In response, Applicants hereby request reconsideration of the application in view of the below-provided remarks. No claims are amended, added, or canceled.

Claim Rejections under 35 U.S.C. 112

Claims 1-12 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. In particular, the Office Action states that it is purportedly unclear how the host controller can copy information to the system memory on the memory bus without being a bus master.

As a preliminary matter, Applicants respectfully note that the Office Action's comments may have paraphrased the language of the claims. However, it should be understood that the language of the claims themselves set out the scope of the claims. Thus, it is noted that the claim language should be viewed in light of the exact language of the claim rather than any paraphrasing or implied limitations asserted by the language employed in the Office Action.

As a matter of clarification, Applicants submit that the copying of information, for example, from an internal memory of the host controller to the system memory does not, in all instances, require the host controller to be a bus master of the system bus. Rather, in some embodiments, the host microprocessor, having access to the internal memory of the host controller, may assist the host controller in copying information from the host controller to the system memory. In another example, the host controller may operate under the control (e.g., as a slave) of the host microprocessor to copy information from the internal memory of the host controller to the system memory. Hence, these exemplary, but non-limiting, embodiments demonstrate that there are ways for the host controller to copy information to the system memory. Applicants respectfully submit that these and/or other exemplary embodiments which facilitate copying information from the host controller to the system memory, without requiring the host controller to be a bus master, are within the scope of the description provided by the specification, including

the subject matter of the claims, and the drawings of the present application. In the alternative, Applicants respectfully submit that this functionality is within the purview of one skilled in the art, given the benefit of the description provided by the present application. Therefore, Applicants submit that the present application provides sufficient detail to describe how the host controller can copy information to the system memory on the memory bus without being a bus master. Accordingly, Applicants respectfully request that the rejections of claims 1-12 under 35 U.S.C. 112, second paragraph, be withdrawn.

Claim Rejections under 35 U.S.C. 102

Claims 1-12 were rejected under 35 U.S.C. 102(a) and 102(b) as being anticipated by Wang et al. (U.S. Pat. Pub. No. 2002/0116565, hereinafter Wang). However, Applicants respectfully submit that these claims are patentable over Wang at least for the reasons provided below.

Independent Claim 1

Claim 1 recites "a first interface for connection to a memory bus which connects the host microprocessor and the system memory, such that the host controller is adapted to act only as a slave on the memory bus" (emphasis added).

In contrast, Wang does not disclose an interface of the host controller for connection to a memory bus. Rather, Wang merely describes a host processor bus 31 which connects the host controller system 100 and, in particular, the host controller logic unit 22 directly to the host microprocessor 24. Wang, Fig. 1A. Although the host microprocessor is separately connected to the system memory 32 via another, unnumbered bus (see the bus between the host microprocessor 24 and the system memory 32 of Fig. 1A), the host processor bus does not connect the host controller system or the host controller logic unit to the memory bus between the host microprocessor and the system memory. In other words, none of the buses shown or described by Wang provides a connection from the host controller system or the host controller logic unit to the memory bus between the host microprocessor and the system memory. The only connection between the host controller system and the system

memory is through the host processor bus, which is connected directly to the host microprocessor. Since Wang does not disclose a connection from the host controller system and the host controller logic to the memory bus between the host microcontroller and the system memory, Wang also fails to disclose an interface of the host controller system for connection to the memory bus between the host microprocessor and the system memory. Therefore, Wang does not disclose all of the limitations of the claim because Wang does not disclose an interface for connection to the memory bus which connects the host microprocessor and the system memory. Accordingly, Applicants respectfully submit that claim 1 is patentable over Wang because Wang does not disclose all of the limitations of the claim.

Independent Claim 10

Applicants respectfully assert independent claim 10 is also patentable over Wang at least for similar reasons to those stated above in regard to the rejection of independent claim 1. In particular, claim 10 recites "a memory bus, which connects the host microprocessor and the system memory" and a host controller comprising "a first interface for connection to the memory bus, such that the host controller is adapted to act only as a slave on the memory bus" (emphasis added).

Here, although the language of claim 10 differs from the language of claim 1 and the scope of claim 10 should be interpreted independently of claim 1, Applicants respectfully assert that the remarks provided above in regard to the rejection of claim 1 also apply to the rejection of claim 10. Accordingly, Applicants respectfully assert claim 10 is patentable over Wang because Wang does not disclose an interface for connection to a memory bus which connects the host microprocessor and the system memory.

Dependent Claims 2-9, 11, and 12

Claims 2-9, 11, and 12 depend from and incorporate all of the limitations of the corresponding independent claims 1 and 10. Applicants respectfully assert claims 2-9, 11, and 12 are allowable based on allowable base claims. Additionally, each of claims 2-9, 11, and 12 may be allowable for further reasons, as described below.

In regard to claim 3, Applicants respectfully submit that claim 3 is patentable over Wang because Wang does not disclose all of the limitations of the claim. Claim 3 recites "wherein the internal memory is a single-port RAM, and the host controller further comprises an arbiter to allow data to be written to and read from the RAM essentially simultaneously" (emphasis added). In contrast, the cited portion of Wang (paragraph 56) merely describes a batch memory with functionality, generally, to allow receiving USB transactions from the host microprocessor for one batch while the host controller system is acting on another batch. However, this description fails to disclose any type of arbiter. Hence, even if the batch memory of Wang were to implement functionality similar to the implementation of the claims, Wang nevertheless fails to disclose all of the individual limitations recited in the claim. In particular, Wang does not disclose all of the limitations of the claim because Wang does not disclose an arbiter. Accordingly, Applicants respectfully assert that claim 3 is patentable over Wang because Wang does not disclose an arbiter, as recited in the claim.

In regard to claim 5, Applicants respectfully submit that claim 5 is also patentable over Wang because Wang does not disclose all of the limitations of the claim. Claim 5 recites "wherein the first part of the internal memory is sub-divided into two sub-parts, and is adapted to store transfer descriptor headers relating to periodic transfers in a first subpart, and to store transfer descriptor headers relating to asynchronous transfers in a second sub-part" (emphasis added). Since claim 5 depends from claim 4, it is appropriate to note that claim 4 recites "wherein the internal memory is divided into two parts, and is adapted to store transfer-based transfer descriptor headers in a first part, and to store transfer-based transfer descriptor payload data in a second part" (emphasis added). In contrast, the cited portions of Wang (paragraphs 62 and 65) merely describe processing batches of USB transactions, generally. However, Wang does not describe a first part of the internal being sub-divided into two sub-parts. In fact, Wang appears to be silent as to storing different types of transfer descriptor headers in different locations within the internal memory of the host controller. Moreover, Wang appears to be silent in regard to storing specific types of transfer descriptor headers relating to periodic transfers and asynchronous transfers. Therefore, Wang does not disclose all of the limitations of the claim because Wang does not disclose an internal memory with a first part sub-divided

into two sub-parts to store transfer descriptor headers relating to periodic transfers and asynchronous transfers, as recited in the claim. Accordingly, Applicants respectfully submit claim 5 is patentable over Wang because Wang does not disclose all of the limitations of the claims.

In regard to claims 8 and 12, Applicants respectfully submit that claims 8 and 12 are also patentable over Wang because Wang does not disclose all of the limitations of the claims. Claim 8 recites "wherein the internal memory is adapted to store multiple micro-frames of transfer descriptors, and to execute the stored transfer descriptors without intervention from the host microprocessor" (emphasis added). Claim 12 recites "wherein the host microprocessor is adapted to write a plurality of micro-frames of transfer descriptors to the system memory and to the host controller, and the host controller is adapted to execute the plurality of micro-frames of transfer descriptors without intervention from the host microprocessor" (emphasis added). In contrast, Wang describes using interrupts to the host microprocessor in order for the host controller system to access the system memory via the memory bus between the host microprocessor and the system memory. Wang, paragraphs 138-140. In other words, the memory accesses between the host controller and the system memory necessarily require the intervention of the host microprocessor because all of the data is transferred to and from the system memory via the host microprocessor. Hence, even if the host microprocessor were to merely forward, or relay, data between the host controller system and the system memory, the host microprocessor nevertheless intervenes at least to a degree in order to facilitate transactions between the host controller system and the system memory. Therefore, Wang does not disclose all of the limitations of the claims because Wang does not disclose executing micro-frames of transfer descriptors without intervention from the host microprocessor, as recited in the claims. Accordingly, Applicants respectfully submit that claims 8 and 12 are patentable over Wang because Wang does not disclose all of the limitations of the claims.

CONCLUSION

Applicants respectfully request reconsideration of the claims in view of the remarks made herein. A notice of allowance is earnestly solicited.

At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-3444** pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees to Deposit Account **50-3444** under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

Respectfully submitted,

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